Lithuanian Journal of Physics, Vol. **47**, No. 4, pp. 451–456 (2007)

DYNAMIC C–V CHARACTERISTICS OF MOS STRUCTURES

S. Sakalauskas [a] and Z. Vaitonis [b]

[a] *Faculty of Physics, Vilnius University, Saulėtekio 9, LT-10222 Vilnius, Lithuania*
[b] *Institute of Materials Science and Applied Research, Vilnius University, Saulėtekio 9, LT-10222 Vilnius, Lithuania*
E-mail: zenonas.vaitonis@ff.vu.lt

Received 23 June 2007; revised 20 September 2007; accepted 21 November 2007

Dynamic C–V characteristics of metal–SiO_2–semiconductor (MOS) structures with p-type semiconductor, made by different technologies, were investigated in this work. Voltage–capacitance characteristics of the structures were measured by linearly varying voltage method. Theoretic and experimental analysis of the method revealed peculiarities of its application. It was determined that dynamic C–V characteristics of the MOS structures have a peak of the capacitance (wider or narrower), its value being higher than capacitance of SiO_2 layer, when the mode of operation changes from depletion to inversion. That character of voltage–capacitance characteristics is determined by redistribution of charge carriers in the heterojunction Si–SiO_2 and recharging rapidity of surface states.

Keywords: linearly varying voltage, MOS structure, C–V characteristics

PACS: 84.37.+q, 73.40.Qv

1. Introduction

Metal–SiO_2–semiconductor structures are widely used in contemporary microelectronics and functional electronics. The production technology of monocrystal silicon wafers has achieved a very high level, but fixed and mobile charges in the SiO_2 layer bring about a lot of problems yet. Mentioned charges significantly change features of heterojunction Si–SiO_2. MOS structure working as a switch or similarly to this mode (e. g. components of computer electronics or visual processing devices) complicates the physical phenomena in the heterojunction and their analysis becomes difficult. It is known [1] that a lot of information about processes in the heterojunction Si–SiO_2 is given by voltage–capacitance (C–V) characteristics measured under the influence of environment (light, heat) or without it. However, it is necessary to note that electrical capacitance of the MOS structure depends on applied voltage value. Therefore we encounter a nonlinear component of capacitance. That is why, in choosing the C–V measurement methods, it is important to pay attention to this feature of the MOS structures. The mentioned effect lets us suppose that measuring the MOS structure dynamic C–V characteristics by using linearly varying voltage source is one of the most universal and operative methods [2].

The aims of this work are to explore the peculiarities of the method for measuring the dynamic C–V characteristics and to estimate its dynamic errors. We also aim to investigate the surface states density and their recharging rapidity in the heterojunction Si–SiO_2 of MOS structures made by different technology by using this method.

2. The peculiarities of dynamic C–V characteristics measurement

Linearly varying voltage source was used for dynamic C–V characteristics registration. The investigated capacitance (MOS structure) and load resistance were inserted into voltage source circuit. The capacitance and the resistor create differentiating RC circuit (Fig. 1).

As mentioned above, the capacitance of the MOS structure depends on voltage, i. e. it is a nonlinear component of capacitance, therefore the current would have two components in the circuit:

$$i(t) = \frac{\mathrm{d}Q_X(t)}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t}\left[C_X(U)\cdot U\right] = \left[C_X(U) + U\frac{\mathrm{d}C_X(U)}{\mathrm{d}U}\right]\frac{\mathrm{d}U}{\mathrm{d}t}\,, \qquad (1)$$

ISSN 1648-8504

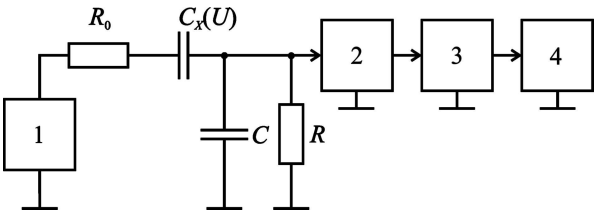

Fig. 1. Installation for measuring the dynamic C–V characteristics. *1* is a linearly varying voltage source, R_0 is its internal resistance, $C_X(U)$ is investigated capacitance, C is parasitic capacitance, R is load resistance, *2* marks a voltage follower, *3* marks an analogue–digital converter, *4* marks a personal computer.

here $Q_X(t)$ is the charge of the investigated capacitor (MOS structure).

It is possible to simplify theoretical analysis of the circuit when Eq. (1) is rewritten for charge of the capacitors in this circuit. Thus we can calculate current $i(t)$ and voltage drop in the resistor R. This voltage is immediately related to he investigated capacitance $C_X(U)$ values. Then, supposed that the value of linearly varying voltage

$$U_0 = \pm\, a \cdot t\,, \tag{2}$$

where a is the rate of linear voltage variation, it is possible to equate:

$$\begin{cases} a \cdot t = R_0 \dfrac{\mathrm{d}Q_X(t)}{\mathrm{d}t} + \dfrac{Q_X(t)}{C_X(U)} + \dfrac{Q(t)}{C}\,, \\ \dfrac{\mathrm{d}Q_X(t)}{\mathrm{d}t} = \dfrac{Q(t)}{RC} + \dfrac{\mathrm{d}Q(t)}{\mathrm{d}t}\,, \end{cases} \tag{3}$$

here $Q(t)$ is the charge of the parasitic capacitor.

The analysis of equation (3) shows that we can eliminate the internal resistance of linearly varying voltage source (it is much less than resistor R resistance) and parasitic capacitance, because it only makes the time constant of measuring circuit $\tau = R[C_X(U) + C]$ bigger, which means that duration of transition process would be longer.

The dependence of MOS structure capacitance on external voltage source is complicated enough [3], that is why we changed theoretical capacitance of the structure in a depletion regime to capacitance of p–n junction depletion layer, which can be easily described and used in experimental research:

$$C_X(U) = \frac{C_0}{\sqrt{\varphi + U}}\,, \tag{4}$$

here φ is electrostatic potential barrier level, U is voltage of external source.

Accepting that the voltage alternation in the investigated structure is linear means that the voltage in load resistor will be much less (this condition is always kept in the experiment). Accordingly, depletion layer capacitance of the p–n junction (in the limited voltage interval) can be described as

$$C_X(U) = C_X(a \cdot t) = C_0\, \mathrm{e}^{-t/\tau_0}\,, \tag{5}$$

here τ is time constant determined experimentally for a concrete diode. Thus the system of equations (3) becomes a simple differential equation

$$\frac{\mathrm{d}Q_X(t)}{\mathrm{d}t} R + \frac{Q_X(t)}{C_0 \mathrm{e}^{-t/\tau_0}} = a \cdot t\,, \tag{6}$$

whose solution is

$$Q_X(t) = \frac{a}{R} \cdot \frac{1}{MN}\left[1 + \frac{N\mathrm{e}^{-tM} - M\mathrm{e}^{-tN}}{M - N}\right],$$

$$M = \frac{1}{2RC_0}\left(1 - \sqrt{\frac{\tau_0 - 4RC_0}{\tau_0}}\right),$$

$$N = \frac{1}{2RC_0}\left(1 + \sqrt{\frac{\tau_0 - 4RC_0}{\tau_0}}\right). \tag{7}$$

Semiconductor diodes were used, whose voltage–capacitance characteristics were measured with high accuracy (the error of measurement was less than $\pm 0.1\%$) and approximated to equation (5), for theoretical verification of results. Then, the charge was calculated with reference to equation (7), and from it the current strength $i(t)$, voltage $U(t)$ in the load resistor, and dynamic capacitance $C_X(U) = C_X(a \cdot t)$ were calculated, too. Experimental and theoretic C–V characteristics of p–n junction are shown in Fig. 2.

The comparison of theoretic and experimental results shows that it is necessary to reduce time constant τ, i. e. to reduce load resistance R, with the purpose of reducing dynamic errors of measurement method. From experimental results it has been established that dynamic errors may be insignificant (about $\pm 1\%$ or less). However, there is still another mode of operation of the MOS structure – an inversion. Capacitance increases very fast in this mode of operation, i. e. by exponential law. But C–V characteristics can depart from this law due to slow recharging of surface states. We have referred to experimental analysis with the intention to exactly describe the increase of structure capacitance. The known capacitance C'' was connected parallel at the chosen time moment to another known capacitance C'. So we could compare theoretic and experimental results correctly. This comparison gave good coincidence. We can see very steep jump of the output voltage in Fig. 3, when capacitance C'' is connected. It is related to preservation (for a very short

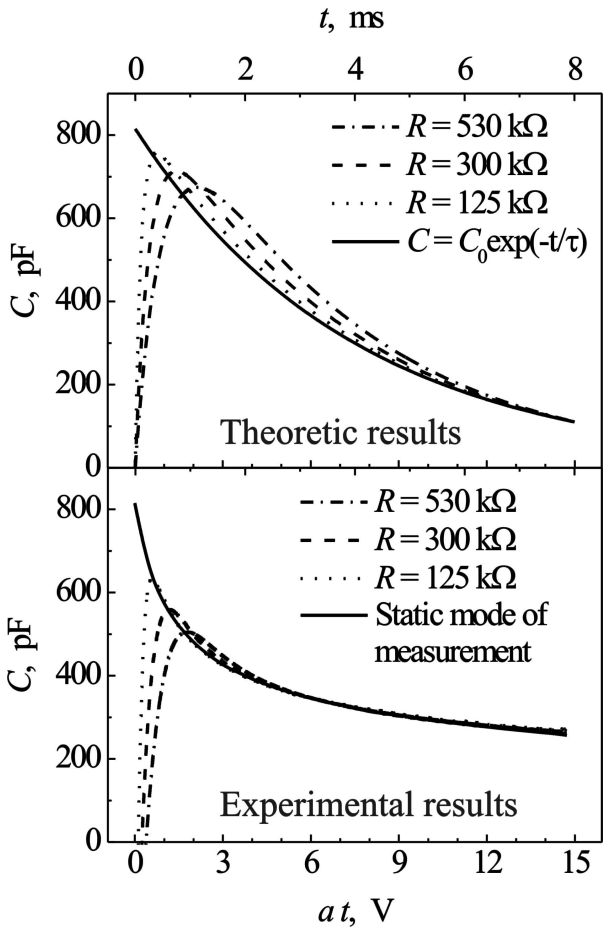

Fig. 2. Experimental and theoretic C–V characteristics of p–n junction.

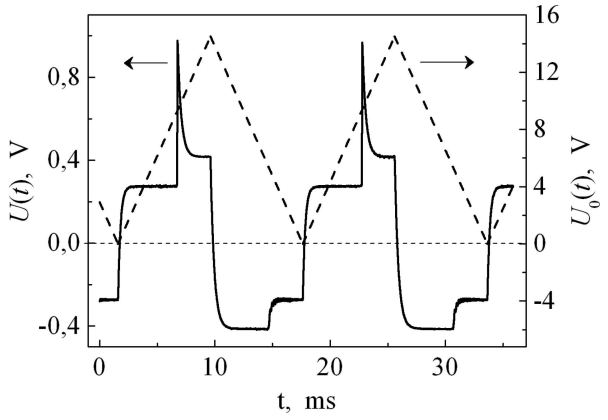

Fig. 3. Experimental results of the measurement, when capacitance increases or decreases saltatorily.

time) of the capacitor C' charge in closed loop of capacitors C' and C'', after commutation. That is why there is no voltage jump, while disconnecting capacitor C''.

After steep voltage jump, the duration of which depends on features of commutator or voltage follower, there starts a transition process with duration equal to

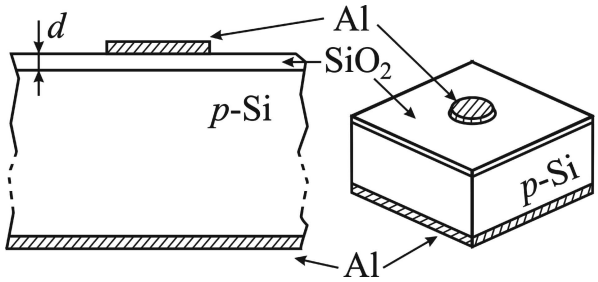

Fig. 4. Structure of investigated samples (d is the thickness of SiO_2 layer).

$(3-5)\cdot R(C' + C'' + C)$. These features of the method we will use in discussion of dynamic C–V characteristics of MOS structures.

3. Formation and experimental investigation of MOS structures

There were two groups of MOS structures formed on p-type (boron doped) monocrystal silicon wafers with specific resistance 10 Ω cm and orientation $\langle 111 \rangle$, investigated experimentally. Structure of the samples is shown in Fig. 4. Silicon dioxide layer was formed by thermal oxidation process in the vapour of different proportions $H_2O : HCl$ solution. Oxidation process of the first MOS structures group proceeds at 1150 °C temperature and thickness of the layer d has been (550±20) nm; for the second group this happens at 1050 °C temperature with oxide thickness (300±15) nm. Field and ohmic contact electrodes were produced from thin Al layer by thermal evaporation in vacuum. Area of the field electrode was less than area of the semiconductor wafer. Company "Altechna" permitted the use of a scanning electron microscope TM 1000 and checked the surface quality of Si wafers and SiO_2 layers grown in different conditions, while the first group of structures was forming. There were no defects detected on the analysed samples. Experimental investigation of MOS structures was made at room temperature in the darkness.

We start the discussion of MOS structures' dynamic C–V characteristics from experimental results shown in Fig. 5. We can see that the capacitance of structure, which is directly proportional to output voltage $U(t)$, increases more than the capacitance of SiO_2 layer, when the surface of semiconductor progresses from accumulation to depletion and later to inversion regime of operation. This phenomenon was observed by other authors [4], but there were no suggestions about capacitance kinetics.

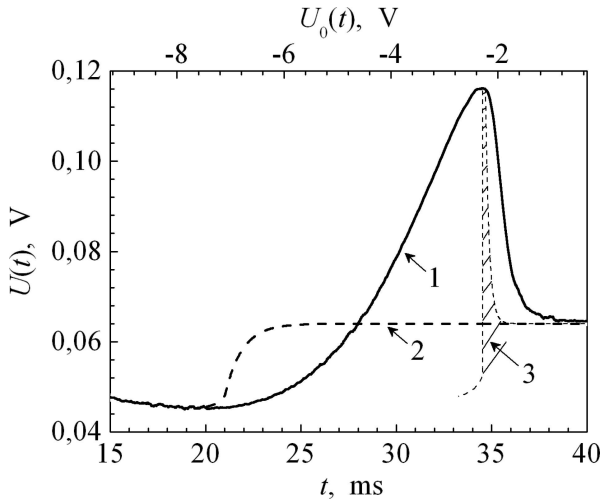

Fig. 5. Typical dynamic C–V characteristics of the MOS structure (p-type semiconductor). *1* is an experimental curve, *2* marks an approximate theoretic capacitance dependence on voltage in transition from depletion to inversion mode of operation, *3* limits the area (lined) determined by dynamic errors of measurement.

From our theoretic and experimental investigation, we want to spotlight that the peak of capacitance induced by dynamic errors of measurement method must take a significantly less area than the measured capacitance (lined area in Fig. 5). This is because the recordable rate of capacitance increase can be very high and only its return to steady state is rather slower. So we can make an assumption that the dynamic measurement errors do not distort the character of transient process and duration if the investigated capacitance is changing not very steeply. Therefore the capacitance kinetics measured by this method and its established peculiarities can give a lot of information about physical features of MOS structures.

Typical dynamic C–V characteristics are shown in Figs. 6 and 7. It is established from Figs. 6(a) and 7 that flat band voltage and equivalent charge in the SiO_2 layer [3] of the first group of samples are significantly greater than those of the second group of MOS structures. It was determined that the speed of recharging of the first group samples is significantly lower than that of the second group ones, and this rapidity also depends on the interval of liner varying voltage (Fig. 6(b)). As mentioned, the area of field electrode is smaller than semiconductor wafer, so it looks like inversion layer at the silicon surface under the electrode can establish itself very fast because of already existing inversion layer around the electrode, produced by a big positive charge in the SiO_2 layer. However, there is no fast flow of electrons to the area under the field electrode. This phenomenon can be explained by a high density of deep states in the heterojunction SiO_2–Si and a slow

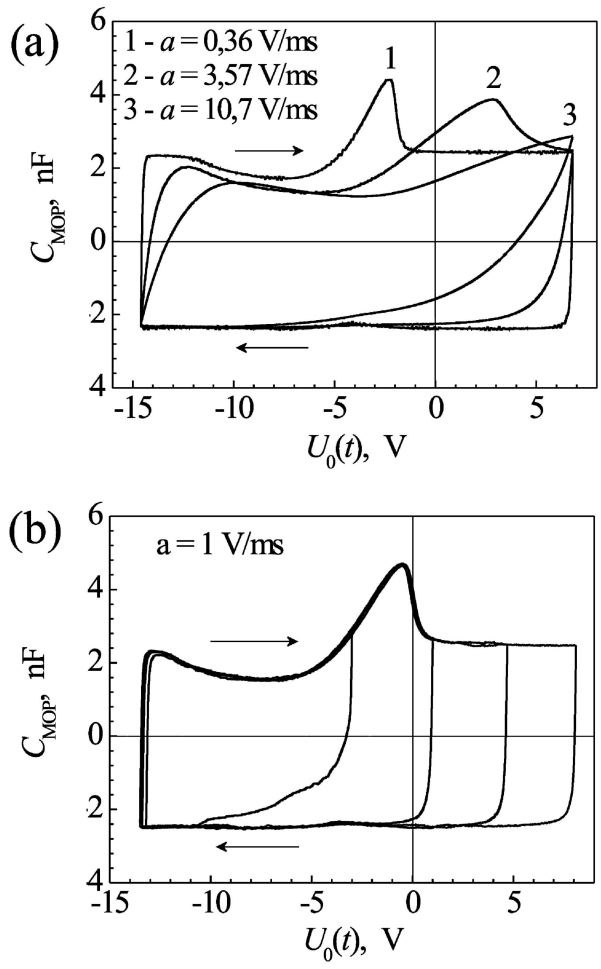

Fig. 6. Dynamic C–V characteristics of the first group of MOS structures: (a) different variation rate of linear voltage, (b) different intervals of linearly varying voltage (arrows show directions of voltage variation).

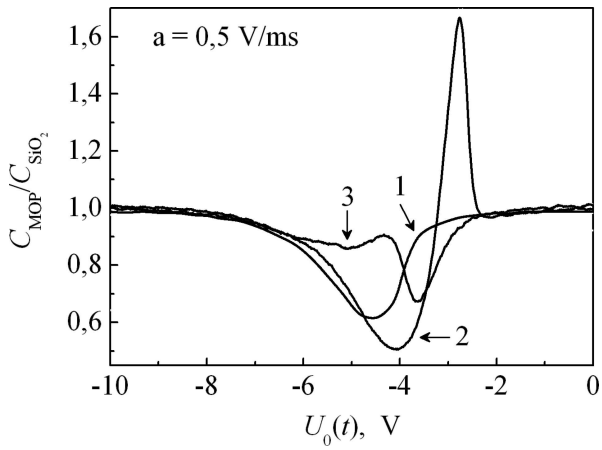

Fig. 7. Dynamic and static (curve *1*) C–V characteristics of the second group of MOS structures (*2* for voltage increase, *3* for voltage decrease).

Table 1. The main calculated parameters of investigated MOS structures.

Parameters	*I* group of the structures	*II* group of the structures
Flat band voltage, V	11.3	6.3
Equivalent charge of the heterojunction, $\mathrm{C/cm^2}$	$(6.9\pm0.1)\cdot10^{-8}$	$(1.5\pm0.1)\cdot10^{-8}$
Surface states density, $\mathrm{cm^{-2}}$	$(4.3\pm0.1)\cdot10^{11}$	$(9\pm1)\cdot10^{10}$

recharging of them [5]. It could be that the following acceptor level is ionized, when high negative voltage is connected to field electrode, i. e. electrons are accumulated in the bulk of semiconductor and in the regions near the field electrode.

4. Discussion of results

Obtained theoretic and experimental results of dynamic C–V characteristics measurement show that the method of investigating capacitance by using linearly varying voltage source warrants very high measurement rapidity and enables one to achieve acceptable level of dynamic errors. A smaller load resistance R, i. e. smaller time constant τ, is necessary to decrease dynamic errors. However, we must note that the ratio between signal and noise then decreases too.

Basic parameters of investigated MOS structures are shown in Table 1. We can see that parameters of the first group of MOS structures, with SiO_2 coating produced by technology of semiconductor devices passivation, are worse than those of the second one. Moreover, formation of the both MOS structure groups in the vapour of $H_2O:HCl$ solution does not give the expected effect, namely, the significant decrease of charge in the heterojunction Si–SiO_2.

Obtained dynamic C–V characteristics of the both MOS structure groups are qualitatively analogous. All of them have peak of capacitance (wider or narrower) with value higher than capacitance of a SiO_2 layer. It shows that a complex recharging process of the slow states in the heterojunction Si–SiO_2 takes place, its rapidity being greater for the second group of MOS structures than for the first one. Electronic conductivity is increased by the electrons afflux from area around field electrode to area under this electrode when mode of operation of the MOS structure changes from depletion to inversion. Evaluation of measured voltage rise in inversion regime of operation lets us discount the thermal generation of minority charge carriers. Probably the afflux of majority charge carriers makes not an exponential barrier, but a significantly complicated one (at the transitional process) at the surface of semiconductor. The mentioned phenomenon explains the investigated peak of MOS structures' capacitance with maximal value exceeding the capacitance of the SiO_2 layer.

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DINAMINĖS MOP DARINIŲ C–V CHARAKTERISTIKOS

S. Sakalauskas, Z. Vaitonis

Vilniaus universitetas, Vilnius, Lietuva

Santrauka

Pateikti skirtingomis technologijomis suformuotų MOP darinių su skylinio laidumo puslaidininkiu dinaminių C–V charakteristikų tyrimo rezultatai. Darinių voltfaradinės charakteristikos buvo matuojamos tiesiškai kintančios įtampos metodu, kurio teorinė ir eksperimentinė analizė atskleidė jo taikymo ypatumus. Tyrimo metu nustatyta, kad MOP darinių dinaminės C–V charakteristikos turi charakteringą talpos smailę (siauresnę ar platesnę), pereinant iš nuskurdinimo į inversinį veikos režimą. Tokį voltfaradinių charakteristikų pobūdį nulemia krūvininkų persiskirstymas nevienalytėje sandūroje Si–SiO_2 ir paviršinių būsenų persielektrinimo sparta.